Patent claims

- 1. A control input circuit (6) for an electrical appliance (1), having a constant current sink (7) which is connected into a control line (2) and whose drawn current (Ia) assumes a detection value (I1) during the length (t1) of a detection pulse (P), whereas the drawn current (Ia) is lowered between two successive detection pulses (P), and also having an evaluation module (15) which analyzes the input current (Ie) flowing in the control line (2) and which indicates a control signal (S) if during the detection pulse (P) the input current (Ie) is not below a prescribed turned-on value for a prescribed turned-on period.
- 2. The control input circuit (6) as claimed in claim 1, characterized in that the constant current sink (7) has an actuation module (13) connected to it which prescribes the magnitude of the drawn current (Ia).
- 3. The control input circuit (6) as claimed in claim 1 or 2, characterized in that the actuation module (13) is an oscillator circuit whose total resistance (RS) alternates discretely between two values.
- 4. The control input circuit (6) as claimed in claim 1 or 2, characterized in that the actuation module (13) comprises a microprocessor (20).
- 5. The control input circuit (6) as claimed in one of claims 1 to 4, characterized in that the constant current sink (7) has a diode (D1) connected upstream of it.
- 6. The control input circuit (6) as claimed in one of claims 1 to 5, characterized in that the evaluation module (15) comprises an RC element (16).

- 7. The control input circuit (6) as claimed in claim 6, characterized in that the RC element (16) has a threshold circuit (17) connected upstream of it which permits a flow of current to the RC element (16) only if the input current (Ie) exceeds the turned-on value.
- 8. The control input circuit (6) as claimed in one of claims 1 to 7, characterized in that the constant current sink (7) comprises a field effect transistor (T1).
- 9. The control input circuit (6) as claimed in one of claims 1 to 8, characterized in that the detection pulses (P) are periodically successive in time.
- 10. The control input circuit (6) as claimed in claim 9, characterized in that when the control signal (S) is in the form of a control voltage (Ust) which alternates over time the period of the detection pulses (P) is coordinated with the phase of the control voltage (Ust).
- 11. The control input circuit (6) as claimed in claim 10, characterized in that a respective detection pulse (P) starts in coordination with each positive half cycle of the control voltage (Ust).
- 12. The control input circuit (6) as claimed in one of claims 1 to 11, characterized in that the drawn current (Ia) of the constant current sink (7) between two successive detection pulses (P) is lowered by at least a factor of 10 in comparison with the detection value (II).
- 13. The control input circuit (6) as claimed in one of claims 1 to 12, characterized in that the turned-on value of the input current (Ie) corresponds to approximately 85% of the detection value (I1).

- 14. The control input circuit (6) as claimed in one of claims 1 to 13, characterized in that the turned-on period is at least 70% of the length (t1) of the detection pulse (P).
- 15. The control input circuit (6) as claimed in one of claims 1 to 14, characterized in that the length (t2) of the period of time between two successive detection pulses (P) exceeds the length (t1) of the or each detection pulse (P) by at least twofold.
- 16. The control input circuit (6) as claimed in one of claims 1 to 15, characterized in that the detection value (I1) is approximately 8 mA.
- 17. The control input circuit (6) as claimed in one of claims 1 to 16, characterized in that the length (t1) of a detection pulse (P) is approximately 4 ms.
- 18. The control input circuit (6) as claimed in one of claims 1 to 17, characterized in that the actuation module (13) and/or the evaluation module (15) are in the form of an integrated circuit.
- 19. An electrical appliance (1) having a control input circuit (6) as claimed in one of claims 1 to 17.